FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
SP015.C16 (1397.028000G)	10/697,257
FIRST NAMED INVENTOR: NGUYEN et al.	
FILING DATE	ART UNIT
October 31, 2003	2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
	AB8						
	AC8						
W	AD8	4,833,599	05/23/1989	Colwell et al.			
W	AE8	4,974,154	11/27/1990	Matsuo			
W	AF8	5,142,634	08/25/1992	Fite et al.			
	AG8						
	AH8						
	AI8						
	AJ8						
	AK8						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL7						Yes No
W	AM7	HEI2-130635	05/18/1990	JP	—	—	X Yes No
	AN7						Yes No
	AO7						Yes No
	AP7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

W	AR	32	Findlay, et al., "HARP: A VLIW RISC Processor", *Proceeding of 5th Annual European Computer Conference on Advanced Computer Technology, Reliable Systems and Applications,* May 16, 1991, pp. 368-372.
W	AS	32	Kuga et al., "DSNS (Dynamically-hazard-resolved, Statically-code-scheduled, Nonuniform Superscalar): Yet Another Superscalar Processor Architecture", Dept. of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Fukuoka, Japan, pp. 14-29.
W	AT	32	Colwell et al., "A VLIW Architecture For A Trace Scheduling Compiler", Association For Computing Machinery (ACM), 1987, pp. 180-192.

EXAMINER [signature] DATE CONSIDERED 08/18/08

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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AT	32	Colwell et al., "A VLIW Architecture For A Trace Scheduling Compiler", Association For Computing Machinery (ACM), 1987, pp. 180-192.

EXAMINER [signature] DATE CONSIDERED 8/1/05

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